### 238P Operating Systems, Fall 2018

### xv6 Boot Recap: Transitioning from 16 bit mode to 32 bit mode

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### what it does

**Sets up** the hardware.

**Transfers** control to the Boot Loader.

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#### how it transfers control to the Boot Loader

Boot loader is loaded from the 1st 512-byte sector of the boot disk.

This 512-byte sector is known as the **boot sector**.

Boot loader is loaded at 0x7c00.

Sets processor's **ip** register to 0x7c00.

### 2 source source files

bootasm.S - 16 and 32 bit assembly code.

bootmain.c - C code.

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bootmain.c - C code.

### executing bootasm.S

- 1. **Disable interrupts** using <u>cli</u> instruction. (<u>Code</u>).
  - > Done in case BIOS has initialized any of its interrupt handlers while setting up the hardware. Also, BIOS is not running anymore, so better to disable them.
  - > Clear segment registers. Use xor for %ax, and copy it to the rest (<u>Code</u>).
- 2. Switch from real mode to protected mode. (References: <u>a</u>, <u>b</u>).
  - > Note the difference between processor modes and kernel privilege modes
  - > We do the above switch to increase the size of the memory we can address.

executing bootasm.S

Let's 2. Switch from real mode to protected mode. expand on this a little bit

### Addressing in Real Mode

In real mode, the processor sends 20-bit addresses to the memory.

(e.g. Intel processors 8086, 8088).

However, it has eight general 16-bit registers + 16 bit segment registers.

How to generate a 20 bit address from a 16 bit register?

Say processor fetches a data read/write instruction.

The processor would then use the data segment register (%ds).

To pass the 16-bit address obtained from %ds to the memory (which accepts 20-bit addresses) we left shift the 16-bit register by 4 bits.

This is equivalent to **adding the register to itself 16 times.** 

(try it out in a bit calculator - e.g. gnu calculator)

Say processor fetches a data read/write instruction.

Use other kinds of segment registers

For example for other kinds of instructions.

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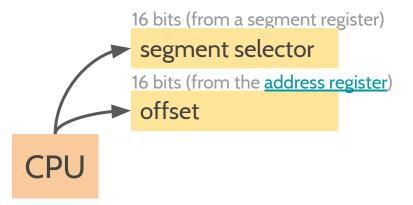
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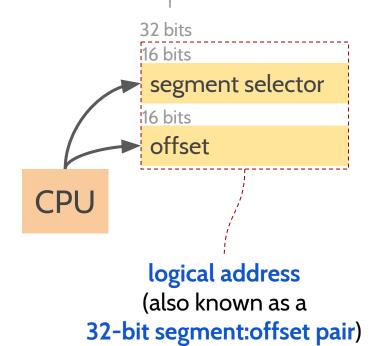
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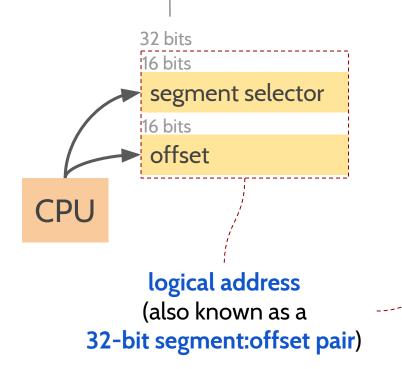
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address translation process takes place in real mode	

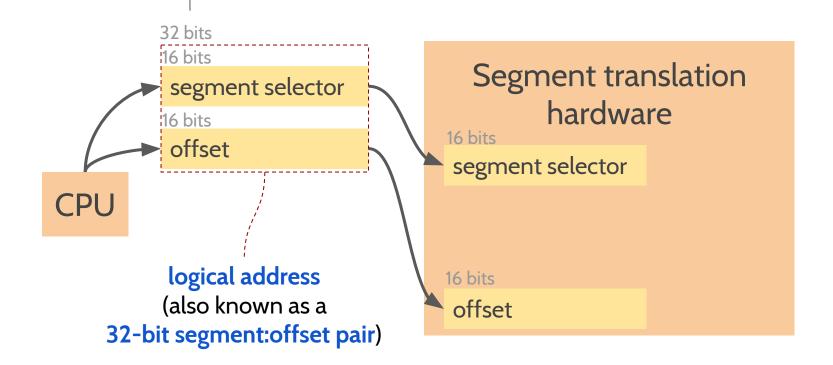
So let's look at how the

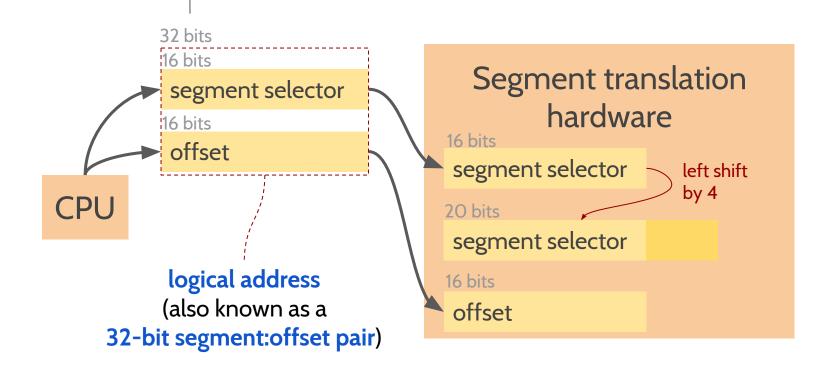


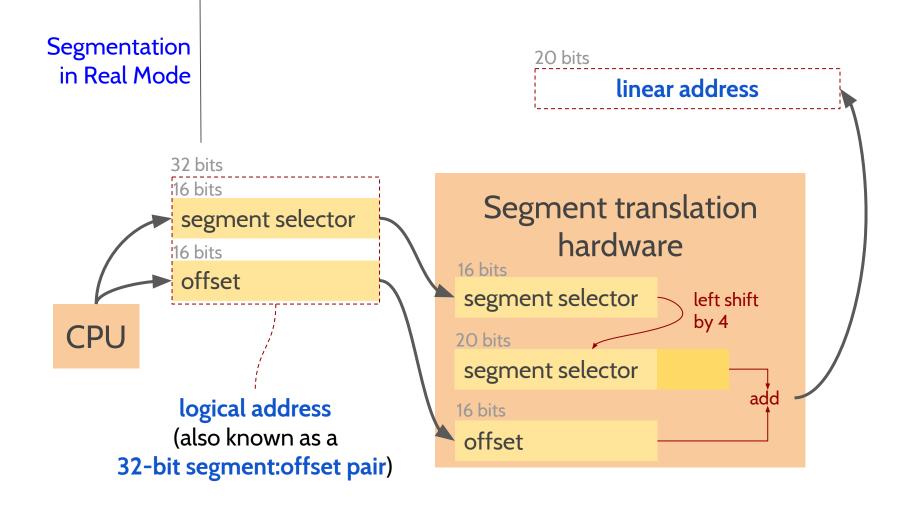


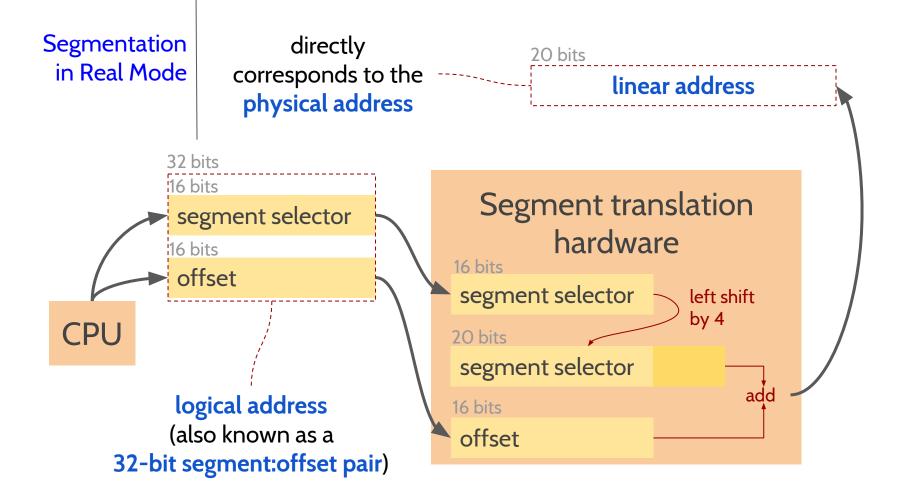


xv6 refers to this x86 logical address as a virtual address





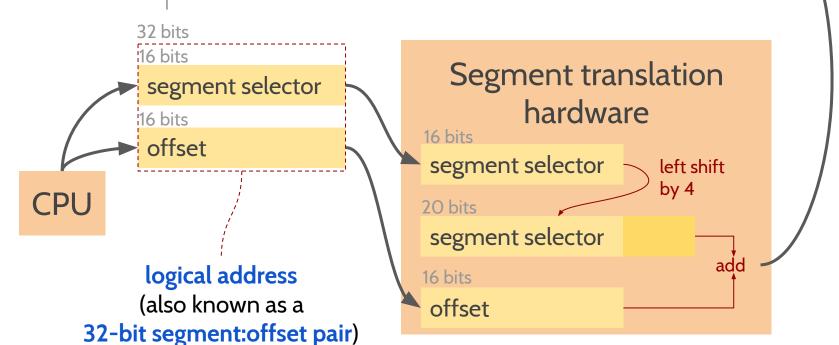




if paging is enabled, this address would go through a further translation process within the paging hardware to generate a physical address



20 bits



linear address



# Segment translation hardware

xv6 configures this hardware such that logical and linear addresses are always the same.

**CPU** 

It follows (without paging) in xv6, logical address

= linear address

= physical address

linear address

logical address

Segment translation hardware

xv6 configures this hardware such that logical and linear addresses are always the same.

Why the switch to Protected Mode?

the maximum size of addressable memory is 2^20 bytes which is **only 1MB**.

With the processor being able to send 20 bit linear addresses,

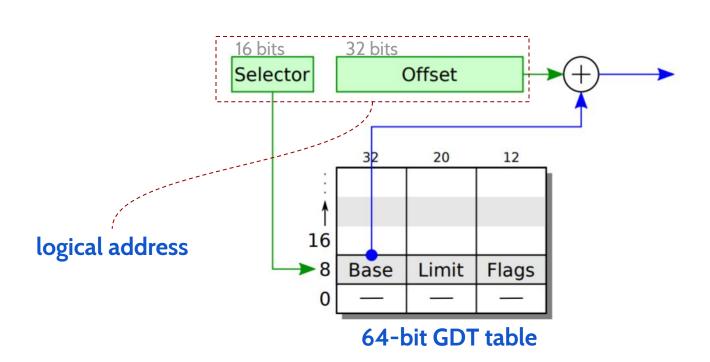
In Protected Mode, the processor can send 32 bit linear addresses, which allows us to address a memory of size 4GB.

Paging hardware is also enabled in Protected Mode.

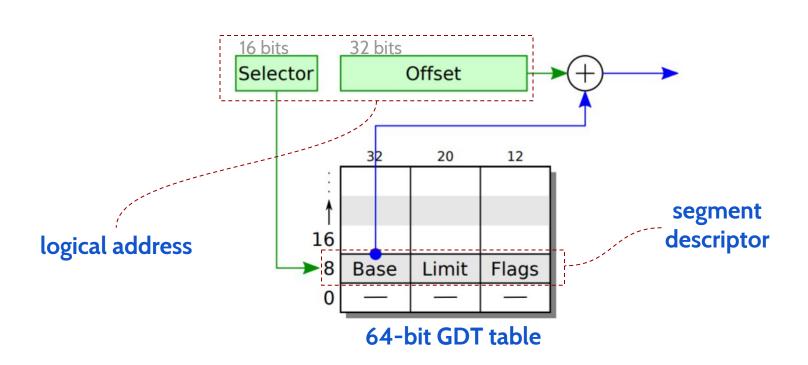
executing bootasm.S

- 2. Switch from real mode to protected mode.
  - > To setup the **protected mode**, the boot loader sets up the **segment descriptor table**, with three entries. Each entry is [a base physical address, max virtual address limit (4GB), permission bits]

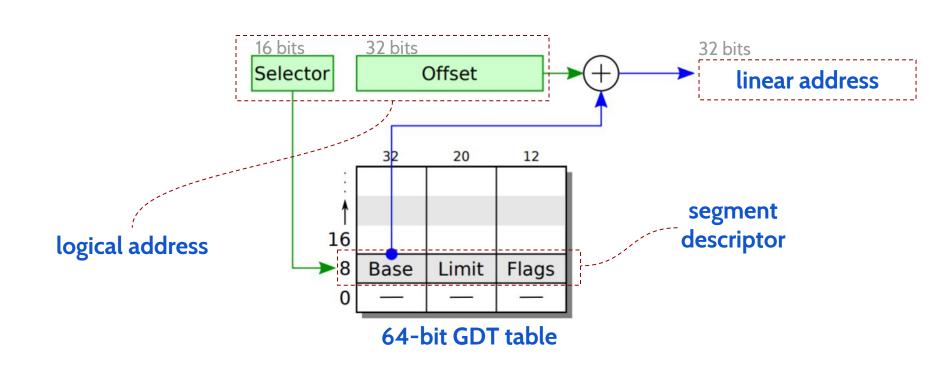
## Segmentation in Protected Mode



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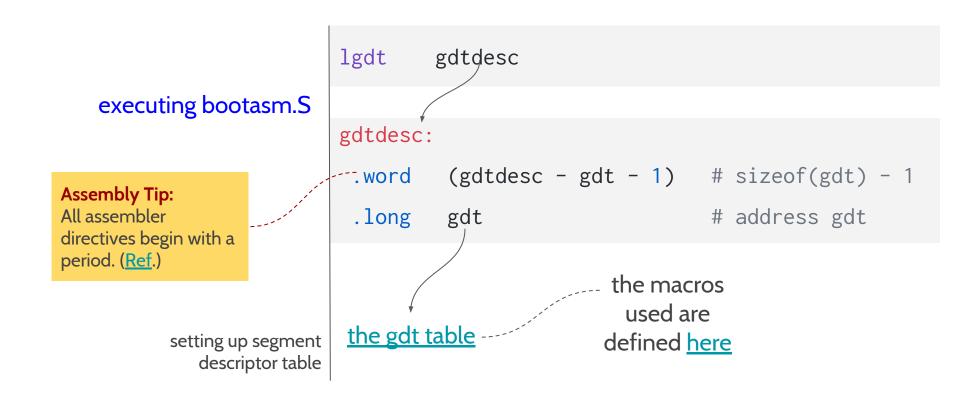
Segmentation in Protected Mode



### executing bootasm.S

```
lgdt
       gdtdesc
gdtdesc:
 .word (gdtdesc - gdt - 1) # sizeof(gdt) - 1
                                # address gdt
 .long
       gdt
                       the macros
                        used are
the gdt table
                      defined here
```

setting up segment descriptor table



executing bootasm.S

- 2. Switch from real mode to protected mode.
  - > Now enable protected mode by setting the 1 bit in control register %crO. (Code).

executing bootasm.S

### 2. Switch from real mode to protected mode.

- > To fully enable protected mode, we need to load a new value into %cs.
- > Since %cs cannot be modified directly we setup %cs here: (code), which results in %cs to refer to the code descriptor entry in gdt.

executing bootasm.S

### **Assembly Tip:**

Long Jump:

ljmp \$0xfebc, \$0x12345678

Use Oxfebc for the CS register and Ox12345678 for the EIP register. (Ref.)

- 2. Switch from real mode to protected mode.
  - > To fully enable protected mode, we need to foad a new value into %cs.
  - > Since %cs cannot be modified directly we 1jmp (code), which results in %cs to refer to the code descriptor entry in gdt (a 32 bit code

seg.)

# We have completed transitioning from 16 bit (real) mode to 32 bit (protected) mode

To see details on how the 32 bit addresses are translated in the segmentation hardware in protected mode look <a href="here">here</a>.

### The next steps in booting....

- bootasm.S makes necessary initializations to call bootmain.c, and calls bootmain
- bootmain loads the kernel into memory

