Virtual Memory and Caches Workout

Discussion 08 - 2 December 2019
CS 250P - Computer Systems Architecture
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Problem 1. Explain how memory virtualization gives a process an illusion of a larger memory.

Solution 1. Anton's Lecture (mins 1:00 to 7:20)

Problem 2. Explain how process isolation is guaranteed by memory virtualization.

Solution 2. Anton's Lecture (mins 1:00 to 7:20)

Problem 3. Say we have a 4GB virtual memory address space for a process, and pages of 4kB each. How big is the translation structure going to be? Assume each entry in the translation structure is 4 bytes.

Solution 3. The number of pages we would need to map is 4GB/4kB = 1 million. Thus we would need to map 1 million entries. Each entry is of size 4 bytes, hence the page translation structure would need to be 4 bytes x 1 million = 4 MB in size.

Problem 4. What's the difference between shared-memory programming model and message passing programming model?

Solution 4. Rajeev's video

Problem 5. What is the value of X in Memory at the end of Cycle 2, given the following sequence of events? Assume we are using a write-back policy.
Cycle 1: Value of X in Cache A is 0, Value of X in Memory is 0.
Cycle 2: CPU updates value of X in Cache B to 1.

Solution 5. 1 (More on cache writing).

Problem 6. Let us take the following sequence of events:
Cycle 1: Value of X in Cache A is 0, Value of X in Cache B is 0. Value of X in Memory is 0.
Cycle 2: CPU-A updates the value of X in Cache A to 1.

a. In the end of cycle-2, what would be the values of X in Cache B, and the memory if we are using a write-update cache coherence policy?
b. In the end of cycle-2, what would be the values of X in Cache B, and the memory if we are using a write-invalidate cache coherence policy?

Solution 6.

a. if using a write-through policy + a write-update cache coherence policy,
   Value of X in cache-B = 1, Value of X in memory = 1
   if using a write-back policy + a write-update cache coherence policy,
   Value of X in cache-B = 1, Value of X in memory = 0
b. if we are using a write-invalidate cache coherence policy
   Both values of X in cache-B and memory would be invalidated

Problem 7. Consider a symmetric shared-memory multiprocessor (3 processors sharing a bus) implementing a snooping cache coherence protocol. For each of the events below, explain the coherence protocol steps (does the cache flag a hit/miss, what request is placed on the bus, who responds, is a writeback required, etc.) and mention the eventual state of the data block in the caches of each of the 3 processors. Assume that the caches are direct-mapped and that each cache line only stores one word and that words X and Y map to the same cache line in each cache (in other words, X and Y cannot both be in the cache at the same time). At the start, X and Y are not in any of the three caches.

P1: Read X

P2: Write X

P2: Read X

P3: Write X

P1: Write X

P1: Read Y

P2: Read X

Solution 7.

Event	P1	P2	P3	Actions
Initial	Inv	Inv	Inv	
P1: Read X	Sh-X	Inv	Inv	P1 has a read miss; a read-request is placed on the bus; memory responds.
P2: Write X	Inv	Excl-X	Inv	P2 has a write miss; a read-excl-request is placed on the bus; memory responds.
P2: Read X	Inv	Excl-X	Inv	P2 has a read hit; no request on the bus.
P3: Write X	Inv	Inv	Excl-X	P3 has a write miss; a read-excl-request is placed on the bus; P2 responds; No writeback to memory.
P1: Write X	Excl-X	Inv	Inv	P1 has a write miss; a read-excl-request is placed on the bus; P3 responds; No writeback to memory.
P1: Read Y	Sh-Y	Inv	Inv	P1 has a read miss for Y; X is written back to memory; read-request for Y is placed on the bus; memory responds.
P2: Read X	Sh-Y	Sh-X	Inv	P2 has a read miss; a read-request for X is placed on the bus; memory responds.

Reference: Anton's (UCI) and Rajeev's (Uni. of Utah) lectures on Computer Architecture