HW1 Solutions

CS250P, Fall 2019,
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Problem 3a: Running instructions in 5-stage pipeline without bypassing

Instructions (gray entries are stalls)	Cycle Number												Comments
	1	2	3	4	5	6	7	8	9	10	11	12	
I1: add r1, r2, r3	IM	REG	ALU	DM	REG/POP(r1)								
I2: lw r4, 4(r4)		IM	REG	ALU	DM	REG/POP(r4)							I2 has no dependency with I1
I3: add r5, r4, r1/STALL			IM	REG/POC(**r1,r4**)	ALU	DM	REG						r1, r4 are not yet produced, so need a stall here
I3: add r5, r4, r1/STALL				IM	REG/POC(r1,**r4**)	ALU	DM	REG					r4 is not yet produced, so need a stall here
I3: add r5, r4, r1					IM	REG/POC(r1,r4)	ALU	DM	REG/POP(r5)				r1, r4 are available (POP of r4, i.e., r4 write, happens in the 1st half of cycle 6, and POC of r4, i.e., r4 read, happens in 2nd half of this cycle)
I4: sw r5, 8(r2)/STALL						IM	REG/POC(**r5**)	ALU	DM	REG			r5 consumed in cycle 7, but not yet produced, stall here
I4: sw r5, 8(r2)/STALL							IM	REG/POC(**r5**)	ALU	DM	REG		r5 consumed in cycle 7, but not yet produced, stall here
I4: sw r5, 8(r2)								IM	REG/POC(r5)	ALU	DM	REG	r5 available

Problem 3b: Running instructions in 5-stage pipeline with bypassing

Instructions (gray entries are stalls)	Cycle Number												Comments
	1	2	3	4	5	6	7	8	9	10	11	12	
I1: add r1, r2, r3	IM	REG	ALU/POP(r1)	DM	REG								
I2: lw r4, 4(r4)		IM	REG	ALU	DM/POP(r4)	REG							I2 has no dependency with I1
I3: add r5, r4, r1/STALL			IM	REG	ALU/POC(**r1,r4**)	DM	REG						r1, r4, are not yet available, stall here
I3: add r5, r4, r1				IM	REG	ALU/POC(r1,r4)	DM	REG					r1, r4 have been produced (available from latches)
I4: sw r5, 8(r2)					IM	REG	ALU	DM/POC(r5)	REG				r5 is consumed at the start of DM stage for I4, cycle 8